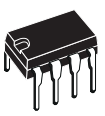
VIPer53DIP
VIPer53SP

OFF LINE PRIMARY SWITCH

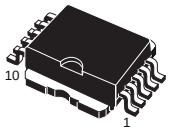
TYPICAL OUTPUT POWER CAPABILITY

Device type	European (195 - 265 Vac)	US / Wide range (85 - 265 Vac)
DIP- 8	50W	30W
PowerSO-10™	65W	40W

Note: 1. Above power capabilities are given under adequate thermal conditions



DIP-8



PowerSO-10™

FEATURES

- SWITCHING FREQUENCY UP TO 300 kHz
- CURRENT LIMITATION
- CURRENT MODE CONTROL WITH ADJUSTABLE LIMITATION
- SOFT START AND SHUT DOWN CONTROL
- AUTOMATIC BURST MODE IN STAND-BY CONDITION (“BLUE ANGEL” COMPLIANT)
- UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- HIGH VOLTAGE STARTUP CURRENT SOURCE
- OVERTEMPERATURE PROTECTION
- OVERLOAD AND SHORT-CIRCUIT CONTROL

DESCRIPTION

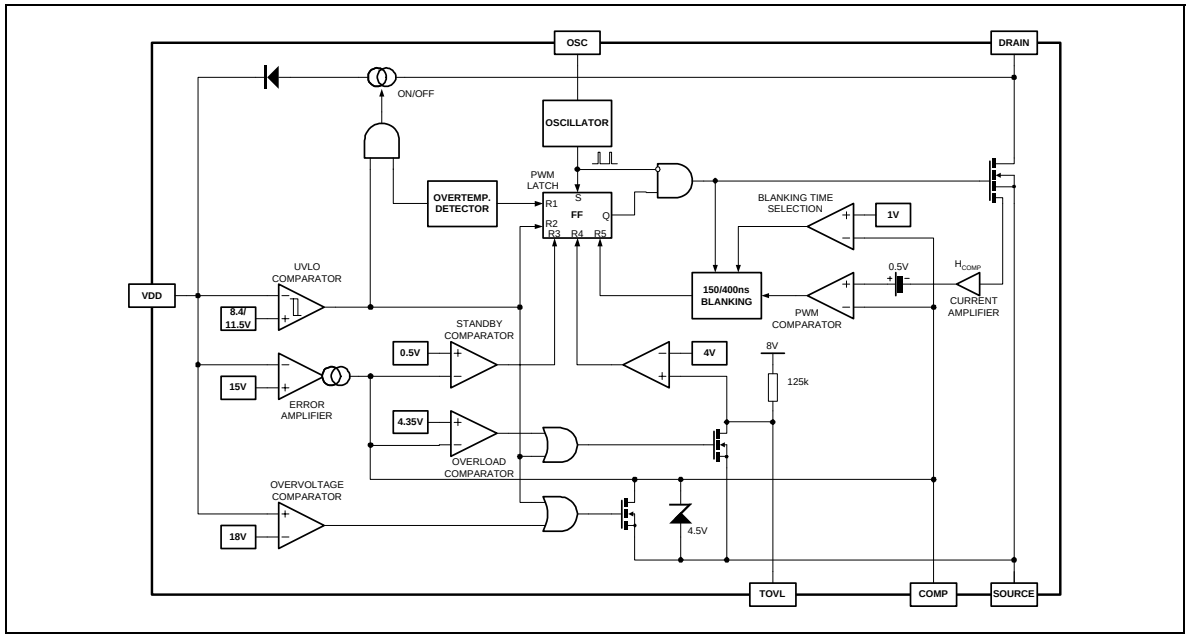
The VIPer53 combines in the same package an enhanced current mode PWM controller with a high voltage MDMesh Power Mosfet. Typical applications cover off line power supplies with a secondary power capability ranging up to 30W in wide range input voltage or 50W in single European voltage range and DIP-8 package, with the following benefits:

– Overload and short circuit controlled by feedback monitoring and delayed device reset.

– Efficient standby mode by enhanced pulse skipping.

– Primary regulation or secondary loop failure protection through high gain error amplifier.

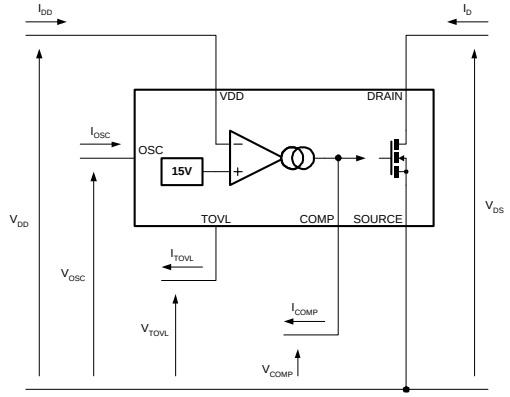
BLOCK DIAGRAM



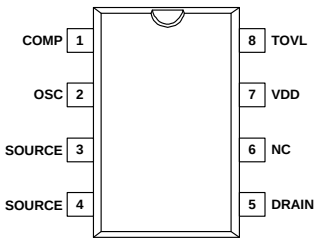
PIN FUNCTION

Name	Function
V_{DD}	Power supply of the control circuits. Also provides the charging current of the external capacitor during startup. The functions of this pin are managed by four threshold voltages: - V_{DDon}: Voltage value at which the device starts switching (Typically 11.5 V). - V_{DDoff}: Voltage value at which the device stops switching (Typically 8.4 V). - V_{DDreg}: Regulation voltage point when working in primary feedback (Trimmed to 15 V). - V_{DDovp}: Triggering voltage of the overvoltage protection (Trimmed to 18 V).
SOURCE	Power Mosfet source and circuit ground reference.
DRAIN	Power Mosfet drain. Also used by the internal high voltage current source during the startup phase, for charging the external V_{DD} capacitor.
COMP	Input of the current mode structure, and output of the internal error amplifier. Allows the setting of the dynamic characteristic of the converter through an external passive network. Useful voltage range extends from 0.5 V to 4.5 V. The Power Mosfet is always off below 0.5 V, and the overload protection is triggered if the voltage exceeds 4.35V. This action is delayed by the timing capacitor connected to the TOVL pin.
TOVL	Allows the connection of an external capacitor for delaying the overload protection, which is triggered by a voltage on the COMP pin higher than 4.35V.
OSC	Allows the setting of the switching frequency through an external Rt-Ct network.

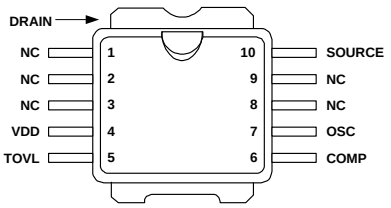
CURRENT AND VOLTAGE CONVENTIONS



CONNECTION DIAGRAM



DIP-8



PowerSO-10™

ORDER CODES

DIP-8	PowerSO-10™		
VIPer53DIP	VIPer53SP		

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Continuous Drain Source Voltage (T_j=25 ... 125°C)	-0.3 ... 620	V
I_D	Continuous Drain Current	Internally limited	A
V_{DD}	Supply Voltage	0 ... 19	V
V_{OSC}	OSC Input Voltage Range	0 ... V_{DD}	V
I_{COMP} I_{TOVL}	COMP and TOVL Input Current Range	-2 ... 2	mA
V_{ESD}	Electrostatic Discharge: Machine Model (R=0Ω; C=200pF) Charged Device Model	 200 1.5	 V kV
T_j	Junction Operating Temperature	Internally limited	°C
T_c	Case Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

THERMAL DATA

Symbol	Parameter		Max Value	Unit
$R_{thj\text{-}case}$	DIP-8		20	°C/W
$R_{thj\text{-}amb}$	DIP-8	(See note 1)	80	°C/W
$R_{thj\text{-}case}$	PowerSO-10™		2	°C/W
$R_{thj\text{-}amb}$	PowerSO-10™	(See note 2)	60	°C/W

Note: 1. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 µm thick) connected to the DRAIN pin.
2. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 µm thick) connected to the device tab.

ELECTRICAL CHARACTERISTICS (T_j=25°C, V_{DD}=13V, unless otherwise specified)

POWER SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Voltage	I_D=1mA; V_{COMP}=0V	620			V
I_{DSS}	Off State Drain Current	V_{DS}=500V; V_{COMP}=0V; T_j=125°C			0.5	mA
$R_{DS(on)}$	Static Drain-Source On State Resistance	I_D=1A; V_{COMP}=4.5V; V_{TOVL}=0V T_j=25°C T_j=100°C		0.9	1 1.7	Ω Ω
t_{fv}	Fall Time	I_D=0.2A; V_{IN}=300V (See figure 1 and note 1)		100		ns
t_{rv}	Rise Time	I_D=1A; V_{IN}=300V (See figure 1 and note 1)		50		ns
C_{oss}	Drain Capacitance	V_{DS}=25V		170		pF
C_{Eon}	Effective Output Capacitance	200V < V_{DSon} < 400V (See note 2)		50		pF

Note: 1. On clamped inductive load

2. This parameter can be used to compute the energy dissipated at turn on E_{ton} according to the initial drain to source voltage V_{DSon} and the following formula : $E_{ton} = \frac{1}{2} \cdot C_{Eon} \cdot V_{DSon}^2$

OSCILLATOR SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{OSC1}	Oscillator Frequency Initial Accuracy	R_T=8kΩ; C_T=2.2nF (See figure 9)	95	100	105	kHz
F_{OSC2}	Oscillator Frequency Total Variation	R_T=8kΩ; C_T=2.2nF (See figure 12) V_{DD}=V_{DDon} ... V_{DDovp}; T_j=0 ... 100°C	93	100	107	kHz
V_{OSChi}	Oscillator Peak Voltage			9		V
V_{OSClo}	Oscillator Valley Voltage			4		V

ELECTRICAL CHARACTERISTICS (T_j=25°C, V_{DD}=13V, unless otherwise specified)

SUPPLY SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DSstart}$	Drain Voltage Starting Threshold	V_{DD}=5V; I_{DD}=0mA		34	50	V
I_{DDch1}	Startup Charging Current	V_{DD}=0 ... 5V; V_{DS}=100V (See figure 2)		-12		mA
I_{DDch2}	Startup Charging Current	V_{DD}=10V; V_{DS}=100V (See figure 2)		-2		mA
$I_{DDchoff}$	Startup Charging Current in Thermal Shutdown	V_{DD}=5V; V_{DS}=100V (See figure 5) $T_j > T_{SD} - T_{HYST}$	0			mA
I_{DD0}	Operating Supply Current Not Switching	F_{sw}=0kHz; V_{COMP}=0V		8	11	mA
I_{DD1}	Operating Supply Current Switching	F_{sw}=100kHz		9		mA
V_{DDoff}	V_{DD} Undervoltage Shutdown Threshold	(See figure 2)	7.5	8.4	9.3	V
V_{DDon}	V_{DD} Startup Threshold	(See figure 2)	10.2	11.5	12.8	V
V_{DDhyst}	V_{DD} Threshold Hysteresis	(See figure 2)	2.6	3.1		V
V_{DDovp}	V_{DD} Overvoltage Shutdown Threshold	(See figure 7)	17	18	19	V

ERROR AMPLIFIER SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DDreg}	V_{DD} Regulation Point	I_{COMP}=0mA (See figure 3)	14.5	15	15.5	V
ΔV_{DDreg}	V_{DD} Regulation Point Total Variation	I_{COMP}=0mA; T_j=0 ... 100°C		2		%
G_{BW}	Unity Gain Bandwidth	From Input =V_{DD} to Output = V_{COMP} I_{COMP}=0mA (See figure 10)		700		kHz
AV_{OL}	Voltage Gain	I_{COMP}=0mA (See figure 10)	40	45		dB
G_m	DC Transconductance	V_{COMP}=2.5V (See figure 3)	1	1.4	1.8	mS
V_{COMPlo}	Output Low Level	I_{COMP}=-0.4mA; V_{DD}=16V		0.2		V
V_{COMPhi}	Output High Level	I_{COMP}=0.4mA; V_{DD}=14V		4.5		V
I_{COMPlo}	Output Sinking Current	V_{COMP}=2.5V; V_{DD}=16V (See figure 3)		-0.6		mA
I_{COMPhi}	Output Sourcing Current	V_{COMP}=2.5V; V_{DD}=14V (See figure 3)		0.6		mA

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_{DD} = 13 V, unless otherwise specified)

PWM COMPARATOR SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
H_{COMP}	ΔV_{COMP} / ΔI_{DPEAK}	V_{COMP}=1 ... 4 V (See figure 8) dI_D/dt=0	1.7	2	2.3	V/A
V_{COMPos}	V_{COMP} Offset	dI_D/dt=0 (See figure 8)		0.5		V
I_{Dlim}	Peak Drain Current Limitation	I_{COMP}=0mA; V_{TOVL}=0V (See figure 8) dI_D/dt=0	1.7	2	2.3	A
I_{Dmax}	Drain Current Capability	V_{COMP}=$V_{COMPovl}$; V_{TOVL}=0V dI_D/dt=0 (See figure 8)	1.6	1.9	2.3	A
t_d	Current Sense Delay to Turn-Off	I_D=1A		250		ns
V_{COMPbl}	V_{COMP} Blanking Time Change Threshold	(See figure 11)		1		V
t_{b1}	Blanking Time	V_{COMP} < V_{COMPBL} (See figure 11)	300	400	500	ns
t_{b2}	Blanking Time	V_{COMP} > V_{COMPBL} (See figure 11)	100	150	200	ns
t_{ONmin1}	Minimum On Time	V_{COMP} < V_{COMPBL}	450	600	750	ns
t_{ONmin2}	Minimum On Time	V_{COMP} > V_{COMPBL}	250	350	450	ns
$V_{COMPoff}$	V_{COMP} Shutdown Threshold	(See figure 6)		0.5		V

OVERLOAD PROTECTION SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{COMPovl}$	V_{COMP} Overload Threshold	I_{TOVL}=0mA (See figure 4 and note 1)		4.35		V
$V_{DIFFovl}$	V_{COMPhi} to $V_{COMPovl}$ Voltage Difference	V_{DD}=V_{DDoff} ... V_{DDreg}; I_{TOVL}=0mA (See figure 4 and note 1)	50	150	250	mV
V_{OVLth}	V_{TOVL} Overload Threshold	(See figure 4)		4		V
t_{OVL}	Overload Delay	C_{OVL}=100nF (See figure 4)		8		ms

Note: 1. $V_{COMPovl}$ is always lower than V_{COMPhi}.

OVERTEMPERATURE PROTECTION SECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{SD}	Thermal Shutdown Temperature	(See fig. 5)	140	160		°C
T_{HYST}	Thermal Shutdown Hysteresis	(See fig. 5)		40		°C

Figure 1: Rise and Fall Time

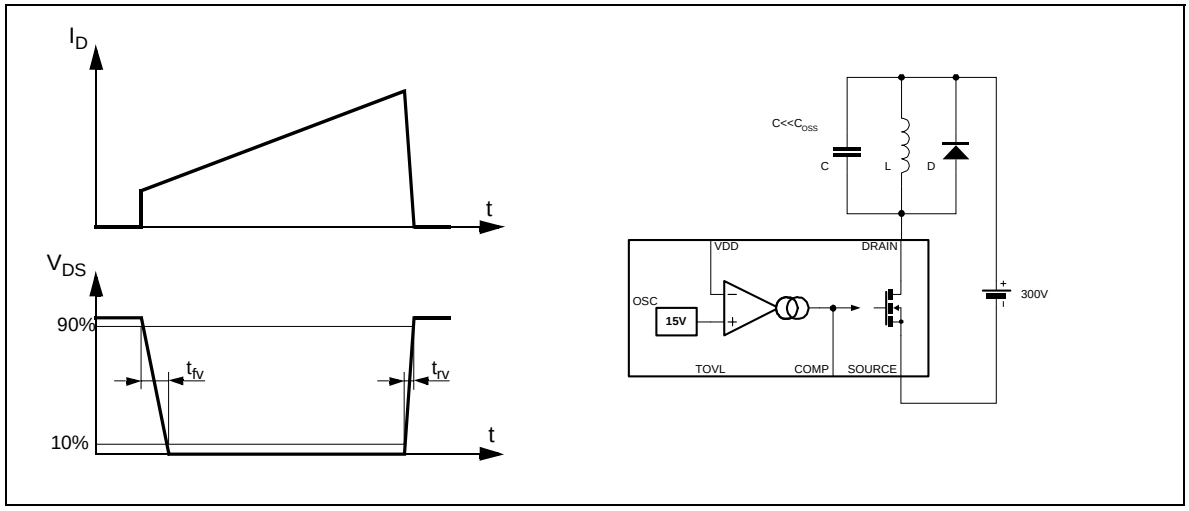


Figure 2: Startup VDD Current

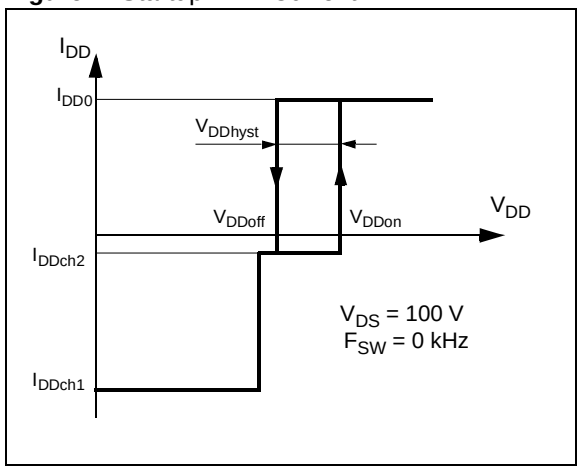


Figure 3: Output Characteristics

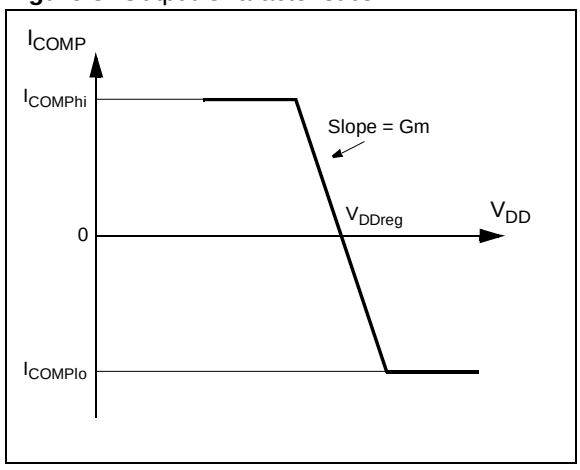


Figure 4: Overload event

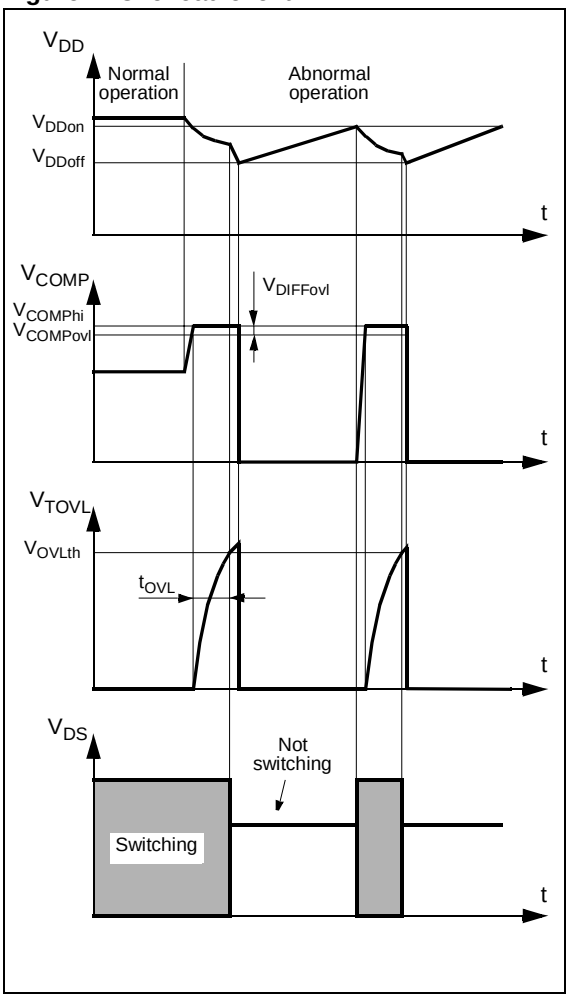


Figure 5: Thermal Shutdown

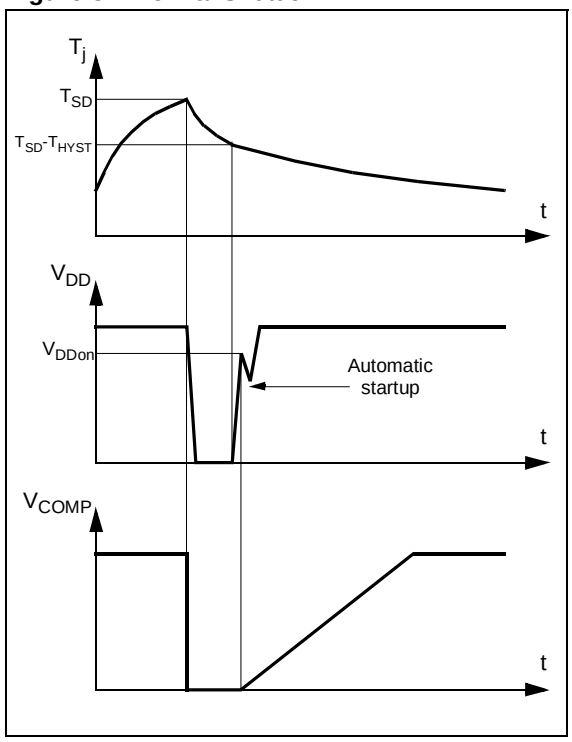


Figure 6: Shut Down Action

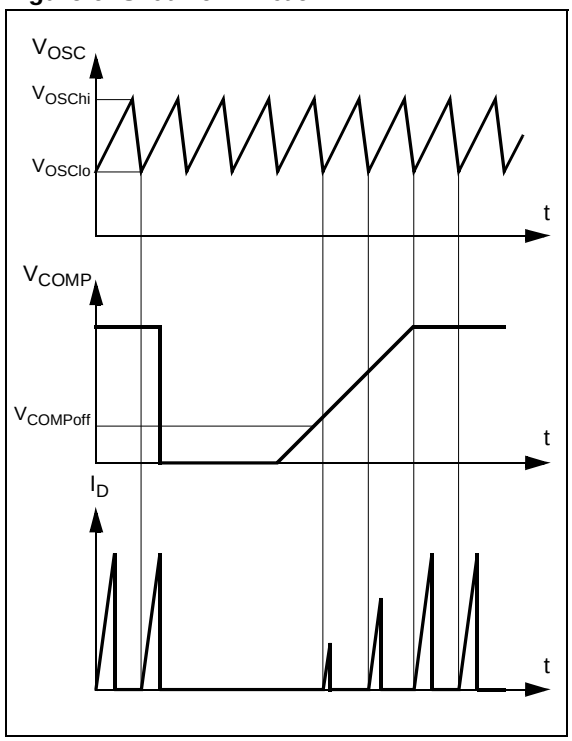


Figure 7: Overvoltage Event

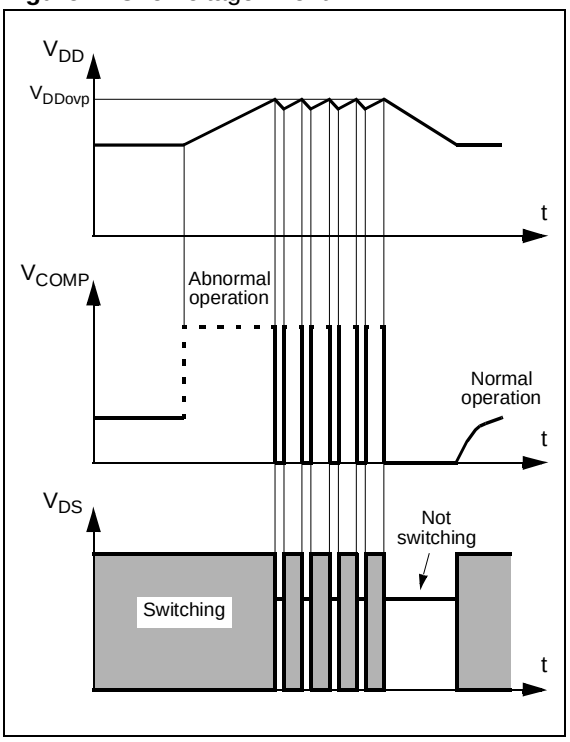


Figure 8: Comp Pin Gain and Offset

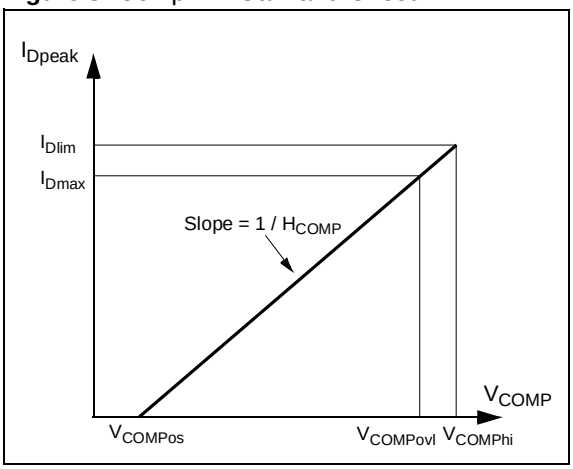
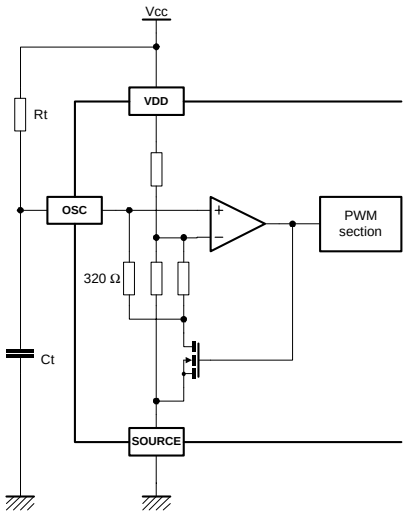


Figure 9: Oscillator Schematic and Settings



The switching frequency settings shown on the graphic here below is valid within the following boundaries:

$R_t > 2k\Omega$

$F_{SW} < 300kHz$

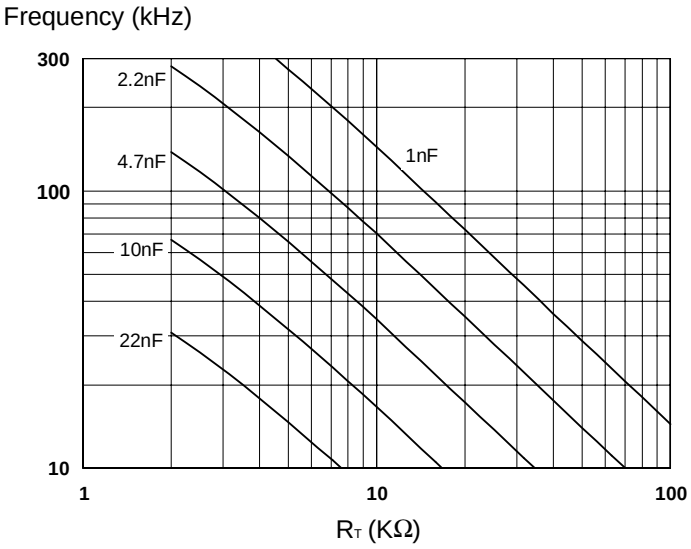


Figure 10: Error Amplifier Transfer Function

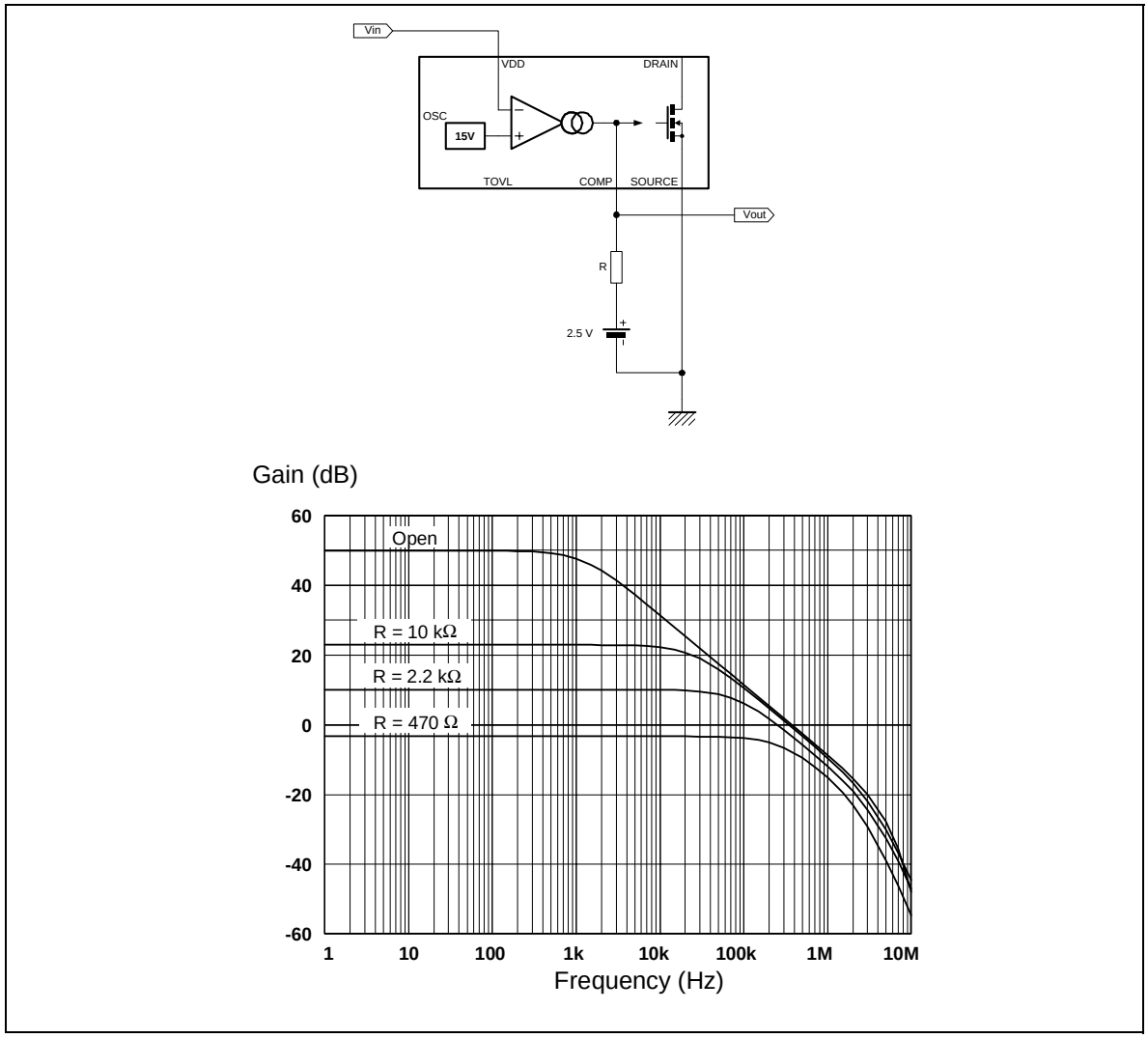


Figure 11: Blanking Time

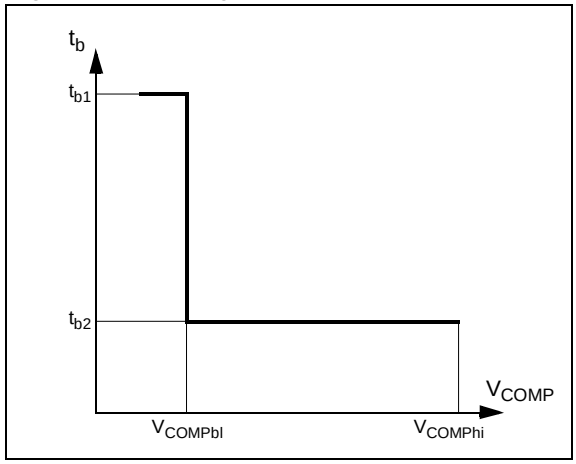


Figure 12: Typical Frequency Variation vs Junction Temperature

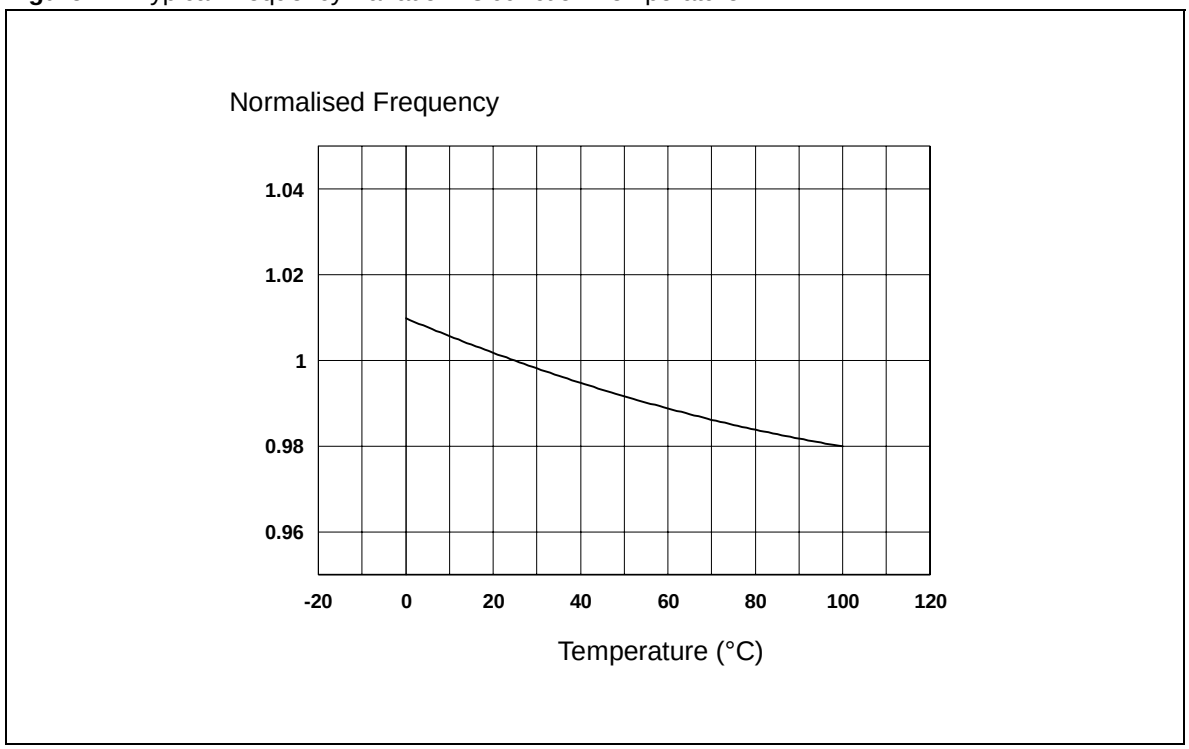


Figure 13: Typical Current Limitation vs Junction Temperature

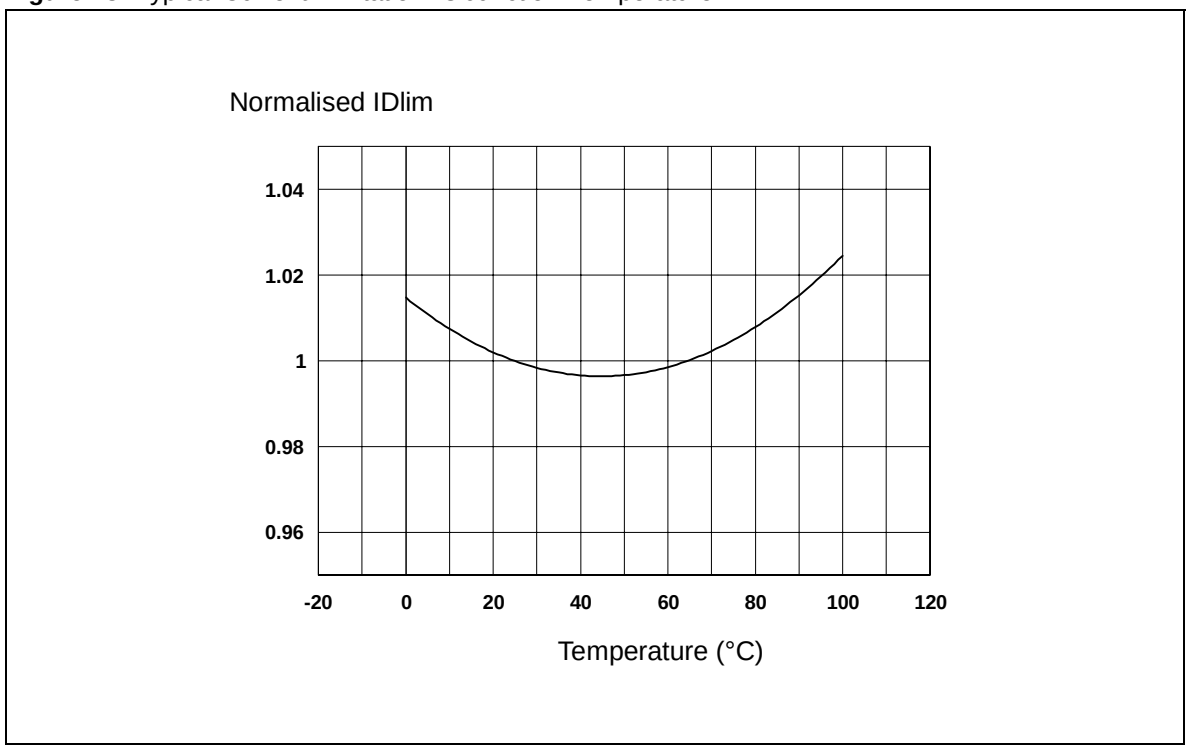
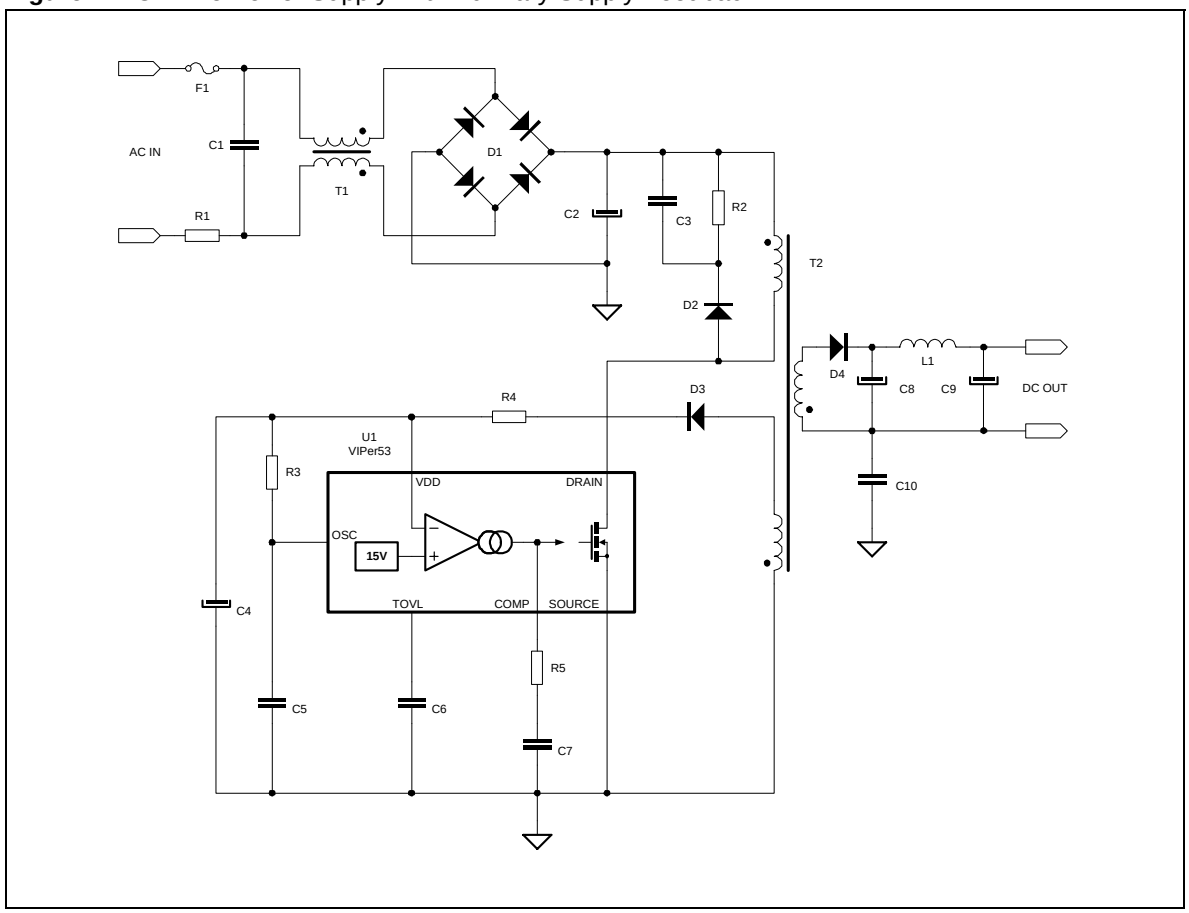


Figure 14: Off Line Power Supply With Auxiliary Supply Feedback



PRIMARY REGULATION CONFIGURATION EXAMPLE

The schematic on figure 14 delivers a fixed output voltage by using the internal error amplifier of the device in a primary feedback configuration. The primary auxiliary winding provides a voltage to the VDD pin, and is automatically regulated at 15 V thanks to the internal error amplifier connected on this pin. The secondary voltage has to be adjusted through the turn ratio of the transformer between auxiliary and secondary.

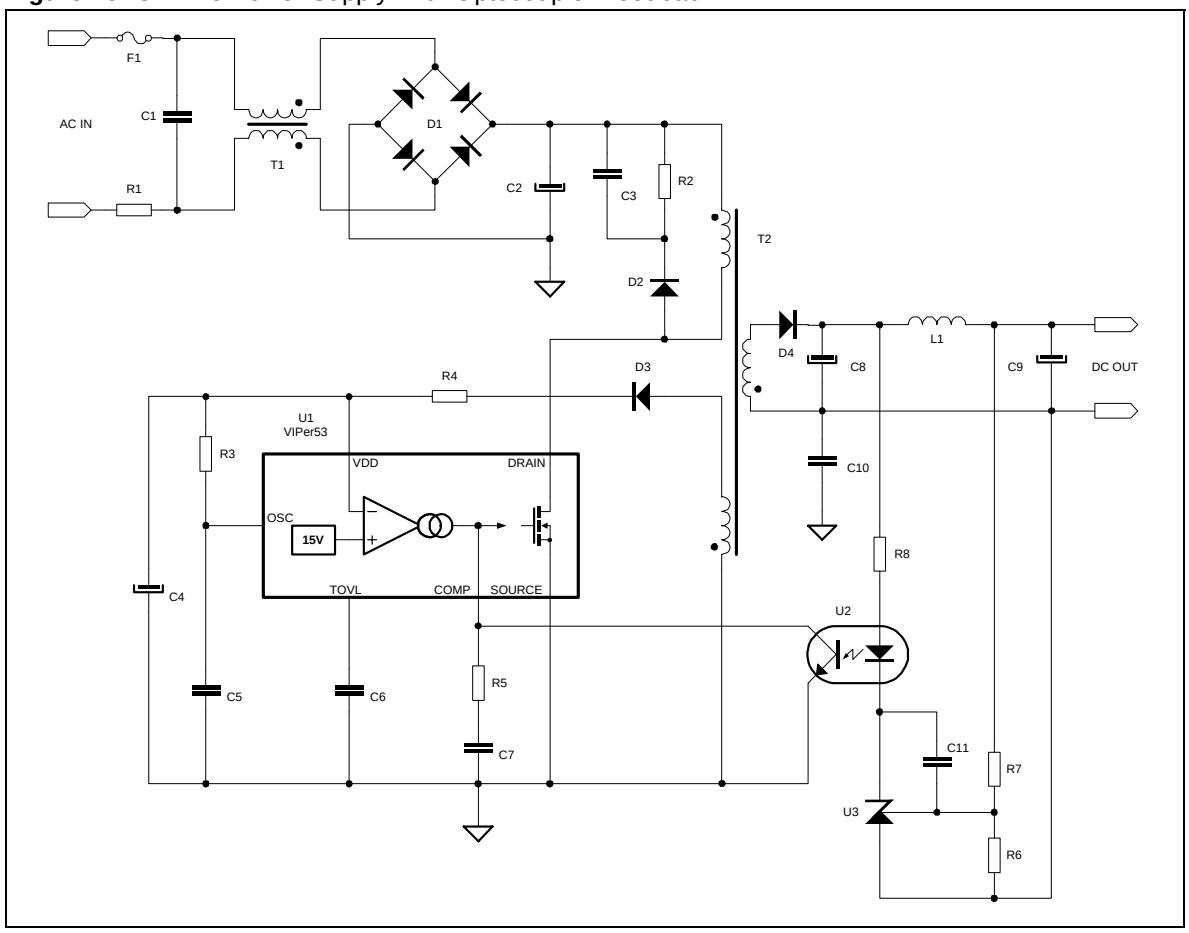
The error amplifier of the VIPer53 is a transconductance one: its output is a current proportional to the difference of voltage between the VDD pin and the internal trimmed 15 V reference, i.e. the error voltage. As the transconductance value is set at a relatively low value to control the overall loop gain and insure stability, this current has to be integrated by a capacitor (C7 in the above schematic). When the steady state operation is reached, this capacitor blocks any DC current from the COMP pin and imposes a nil error voltage. Therefore, the V_{DD} voltage is accurately regulated to 15 V.

This results in a good load regulation, which depends only on transformer coupling and output diodes impedance. The current mode structure takes care of all incoming voltage changes, thus providing at the same time an excellent line regulation.

The switching frequency can be set to any value through the choice of R3 and C5. This allows to optimize the efficiency of the converter by adopting the best compromise between switching losses, EMI (Lower with low switching frequencies) and transformer size (Smaller with high switching frequencies). For an output power of a few watts, typical switching frequencies are comprised between 20 kHz and 40 kHz because of the small size of the transformer. For higher power, 70 kHz to 130 kHz are generally chosen.

The value of the compensation resistor R5 sets the dynamic behavior of the converter. It can be adjusted to provide the best compromise between stability and recovering time with fast load changes.

Figure 15: Off Line Power Supply With Optocoupler Feedback



SECONDARY FEEDBACK CONFIGURATION EXAMPLE

When a more accurate output voltage is needed, the definitive way is to monitor it directly on secondary side, and to drive the PWM controller through an optocoupler as shown on figure 15.

The optocoupler is connected in parallel with the compensation network on the COMP pin. The design of the auxiliary winding will be made in such a way that the V_{DD} voltage is always lower than the internal 15 V reference. The internal error amplifier will therefore be saturated in the high state, and because of its transconductance nature, will deliver a constant biasing current of 0.6 mA to the optotransistor. This current doesn't depend on the compensation voltage, and so it doesn't depend on the output load either. The gain of the optocoupler ensures consequently a constant biasing of the TL431 device (U3) which is in charge of secondary regulation. If the optocoupler gain is sufficiently low, no additional components are required to ensure a minimum current biasing of U3. Also, the low biasing current value avoid any ageing of the optocoupler.

The constant current biasing can be used to simplify the secondary circuit: Instead of a TL431, a simple zener and resistance network in series with the optocoupler diode can insure a good secondary regulation. As the current flowing in this branch remains constant for the same reason as above, typical load regulation of 1% can be achieved from zero to full output current with this simple configuration.

Since the dynamic characteristics of the converter are set on the secondary side through components associated to U3, the compensation network has only a role of gain stabilization for the optocoupler, and its value can be freely chosen. R5 can be set to a fixed value of 1 kΩ, offering the possibility of using C7 as a soft start capacitor: When starting up the converter, the VIPer53 device delivers a constant current of 0.6 mA on the COMP pin, creating a constant voltage of 0.6 V in R5 and a rising slope across C7. This voltage shape together with the operating range of 0.5 V to 4.5 V

provides a soft startup of the converter. The rising speed of the output voltage can be set through the value of C7. C4 and C6 values must be adjusted accordingly in order to ensure a correct startup.

CURRENT MODE TOPOLOGY

The VIPer53 implements the conventional current mode control method for regulating the output voltage. This kind of feedback includes two nested regulation loops:

The inner loop controls the peak primary current cycle by cycle. When the Power MOSFET output transistor is on, the inductor current (primary side of the transformer) is monitored with a SenseFET technique and converted into a voltage Vs. When Vs reaches V_{COMP}, the power switch is turned off. This structure is completely integrated as shown on the Block Diagram of page 1, with the current amplifier, the PWM comparator, the blanking time function and the PWM latch. The following formula gives the peak current in the Power MOSFET according to the compensation voltage:

$$I_{Dpeak} = \frac{V_{COMP} - V_{COMPos}}{H_{COMP}}$$

The outer loop defines the level at which the inner loop regulates peak current in the power switch. For this purpose, V_{COMP} is driven by the output of the error amplifier (Either the internal one in primary feedback configuration or a TL431 through an optocoupler in secondary feedback configuration, see figures 14 and 15) and is set accordingly the peak drain current for each switching cycle.

As the inner loop regulates the peak primary current in the primary side of the transformer, all input voltage changes are compensated for before impacting the output voltage. This results in an improved line regulation, instantaneous correction to line changes and better stability for the voltage regulation loop.

Current mode topology also provides a good converter startup control. As the compensation voltage can be controlled to increase slowly during the startup phase, the peak primary current will follow this soft voltage slope to provide a smooth output voltage rise, without any overshoot. The simpler voltage mode structure which only controls the duty cycle, leads generally to high currents at startup with the risk of transformer saturation. The compensation pin can also be used to limit the current capability of the device (See Current Limitation section).

An integrated blanking filter inhibits the PWM comparator output for a short time after the integrated Power MOSFET is switched on. This function prevents anomalous or premature termination of the switching pulse in the case of current spikes caused by primary side transformer capacitance or secondary side rectifier reverse recovery time when working in continuous mode.

STANDBY MODE

The device implements a special feature to address the low load condition. The corresponding function described hereafter consists of reducing the switching frequency by going into burst mode, with the following benefits:

– It reduces the switching losses, thus providing low consumption on the mains lines. The device is compliant with “Blue Angel” and other similar standards, requiring less than 0.5 W of input power when in standby.

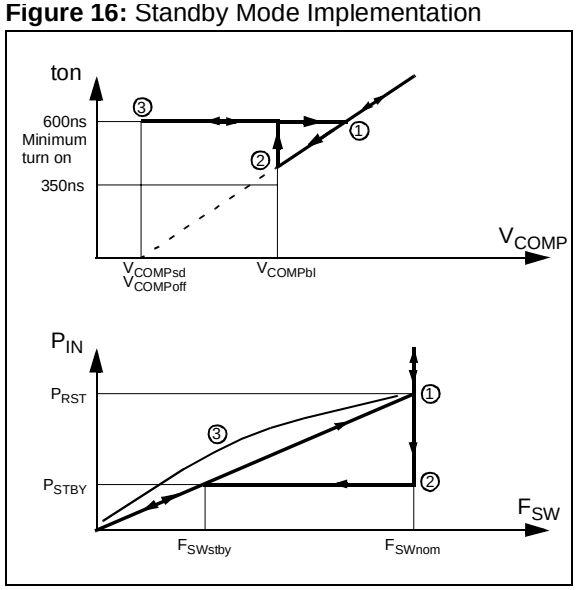
– It allows the regulation of the output voltage, even if the load corresponds to a duty cycle that the device is not able to generate because of the internal blanking time, and associated minimum turn on.

For this purpose, a comparator monitores the COMP pin voltage, and maintains the PWM latch and the Power MOSFET in the off state as long as V_{COMP} remains below 0.5 V (See Block Diagram on page 1). If the output load requires a duty cycle below the one defined by the minimum turn on of the device, the error amplifier decreases its output voltage until it reaches this 0.5 V threshold ($V_{COMPoff}$). The Power MOSFET can be completely off for some cycles, and resumes normal operation as soon as V_{COMP} is higher than 0.5 V. The output voltage is regulated in burst mode. The corresponding ripple is not higher than the nominal one at full load.

In addition, the minimum turn on time which defines the frontier between normal operation and burst mode changes according to V_{COMP} value. Below 1 V (V_{COMPbl}), the blanking time increases to 400 ns, whereas it is 150 ns for higher voltages (See figure 11). The minimum turn on times resulting from these values are respectively 600 ns and 350 ns, when taking into account internal propagation time. This brutal change induces an hysteresis between normal operation and burst mode as shown on figure 16.

When the output power decreases, the system reaches point 2 where V_{COMP} equals V_{COMPbl}. The minimum turn on time passes immediately from 350 ns to 600 ns, exceeding the effective turn on time that should be needed at such output power level. Therefore the regulation loop will quickly drive V_{COMP} to $V_{COMPoff}$ (Point 3) in order to pass into burst mode and to control the output voltage. The corresponding hysteresis can be seen on the switching frequency which passes from F_{SWnom} which is the normal switching frequency set by the components connected to the OSC pin, to F_{SWstby}. Note that this frequency is

Figure 16: Standby Mode Implementation



actually an equivalent number of switching pulses per second, rather than a fixed switching frequency, as the device is working in burst mode.

As long as the power remains below P_{RST} the output of the regulation loop remains stuck at V_{COMPsd} and the converter works in burst mode. Its "density" increases (i.e. the number of missing cycles decreases) as the power approaches P_{RST} and resumes finally normal operation at point 1. The hysteresis cannot be seen on the switching frequency, but the COMP pin voltage which passes brutally at that power level from point 3 to point 1.

The power points value P_{RST} and P_{STBY} are defined by the following formulas:

$$P_{RST} = \frac{1}{2} \cdot F_{SWnom} \cdot (tb_1 + td)^2 \cdot V_{IN}^2 \cdot \frac{1}{Lp}$$

$$P_{STBY} = \frac{1}{2} \cdot F_{SWnom} \cdot Ip^2(V_{COMPbl}) \cdot Lp$$

Where $Ip(V_{COMPbl})$ is the peak Power MOSFET current corresponding to a compensation voltage of V_{COMPbl} (1V), that is to say about 250 mA. Note that the power point P_{STBY} where the converter is going into burst mode doesn't depend on the input voltage.

The standby frequency $F_{SWstb\ y}$ is given by:

$$F_{SWstby} = \frac{P_{STBY}}{P_{RST}} \cdot F_{SWnom}$$

The ratio between the nominal switching frequency and the standby one can be as high as 4, depending on the Lp value and input voltage.

HIGH VOLTAGE STARTUP CURRENT SOURCE

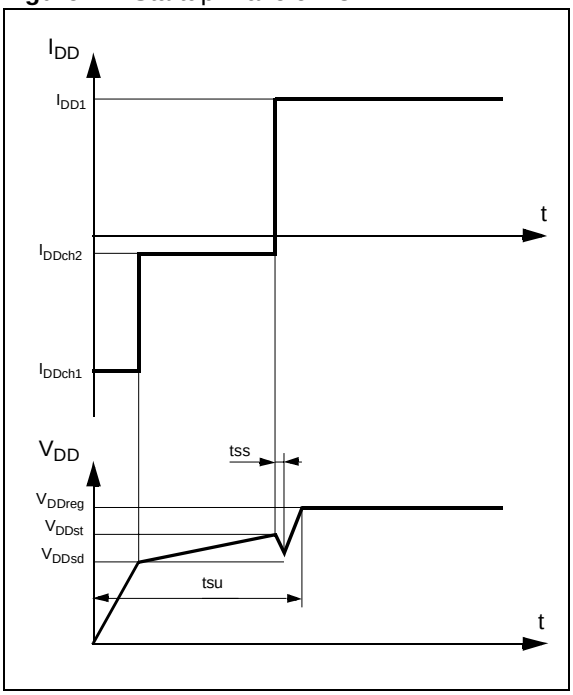
An integrated high voltage current source provides a bias current from the DRAIN pin during the startup phase. This current is partially absorbed by internal control circuits in standby mode with reduced consumption and also supplies the external capacitor connected to the VDD pin. As soon as the voltage on this pin reaches the high voltage threshold V_{DDon} of the UVLO logic, the device turns into active mode and starts switching. The startup current generator is switched off, and the converter should normally provide the needed current on the VDD pin through the auxiliary winding of the transformer, as shown on figure 14 or 15.

The external capacitor C_{VDD} on the VDD pin must be sized according to the time needed by the converter to startup, when the device starts switching. This time tss depends on many parameters, among which transformer design, output capacitors, soft start feature and compensation network implemented on the COMP pin and possible secondary feedback circuit. The following formula can be used for defining the minimum capacitor needed:

$$C_{VDD} > \frac{I_{DD1} \cdot tss}{V_{DDhyst}}$$

Figure 17 shows a typical startup event. V_{DD} starts from 0 V with a charging current I_{DDch1} at about 9 mA. When about V_{DDoff} is reached, the charging current is reduced down to I_{DDch2} which is about

Figure 17: Startup Waveforms



0.6 mA. This lower current leads to a slope change on the V_{DD} rise. The device starts switching for a V_{DD} equal to V_{DDon}, and the auxiliary winding delivers some energy to the V_{DD} capacitor after the startup time tss.

The charging current change at V_{DDoff} allows a fast complete startup time tsu, and maintains a low restart duty cycle. This is especially useful for short circuits and overloads conditions, as described in the following section.

SHORT-CIRCUIT AND OVERLOAD PROTECTION

A $V_{COMPovl}$ threshold of about 4.35 V has been implemented on the COMP pin. When V_{COMP} goes above this level, the capacitor connected on the TOVL pin begins to charge. When reaching typically 4 V (V_{OVLth}), the internal mosfet driver is disabled and the device stops switching. This state is latched thanks to the regulation loop which maintains the COMP pin voltage above the $V_{COMPovl}$ threshold. Since the VDD pin doesn't receive any more energy from the auxiliary winding, its voltage drops down until it reaches VDDoff and the device is reset, recharging the VDD capacitor for a new restart cycle. Note that if VCOMP drops down below the $V_{COMPovl}$ threshold for any reason during the VDD drop, the device resumes switching immediately.

The device enters an endless restart sequence if the overload or short circuit condition is maintained. The restart duty cycle D_{RST} is defined as the time ratio for which the device tries to restart, thus delivering its full power capability to the output. In order to keep the whole converter in a safe state during this event, D_{RST} must be kept as low as possible, without compromising the real start up of the converter. A typical value of about 10 % is generally sufficient. For this purpose, both VDD and TOVL capacitors can be used to satisfy the following conditions:

$$C_{OVL} > 12.5 \cdot 10^{-6} \cdot tss$$

$$C_{VDD} > 8 \cdot 10^{4} \cdot \left(\frac{1}{D_{RST}} - 1\right) \cdot \frac{C_{OVL} \cdot I_{DDch2}}{V_{DDhyst}}$$

Refer to the previous startup section for the definition of tss, and C_{VDD} must also be checked against the limit given in this section. The maximum value of the two calculus will be adopted.

All this behavior can be observed on figure 4. In Figure 8 the value of the drain current Id for V_{COMP}=$V_{COMPovl}$ is shown. The corresponding parameter I_{Dmax} is the drain current to take into account for design purpose. Since I_{Dmax} represents the maximum value for which the overload protection is not triggered, it defines the power capability of the power supply.

TRANSCONDUCTANCE ERROR AMPLIFIER

The VIPer53 includes a transconductance error amplifier. Transconductance Gm is the change in output current I_{COMP} versus change in input voltage V_{DD}. Thus:

$$Gm = \frac{\partial I_{COMP}}{\partial V_{DD}}$$

The output impedance Z_{COMP} at the output of this amplifier (COMP pin) can be defined as:

$$Z_{COMP} = \frac{\partial V_{COMP}}{\partial I_{COMP}} = \frac{1}{Gm} \cdot \frac{\partial V_{COMP}}{\partial V_{DD}}$$

This last equation shows that the open loop gain A_{VOL} can be related to Gm and Z_{COMP}:

$$A_{VOL} = Gm \cdot Z_{COMP}$$

where Gm value for VIPer53 is typically 1.4 mA/V.

Gm is well defined by specification, but Z_{COMP} and therefore A_{VOL} are subject to large tolerances. An impedance Z must be connected between the COMP pin and ground in order to define accurately the transfer function F of the error amplifier, according to the following equation, very similar to the one above:

$$F(p) = Gm \cdot Z(p)$$

The error amplifier frequency response is shown in figure 10 for different values of a simple resistance connected on the COMP pin. The unloaded transconductance error amplifier shows an internal Z_{COMP} of about 140 KΩ. More complex impedances can be connected on the COMP pin to achieve different compensation methods. A capacitor provides an integrator function, thus eliminating the DC static error, and a resistance in series leads to a flat gain at higher frequency, introducing a zero and ensuring a correct phase margin. This configuration is illustrated in figure 18 for the schematic and figure 19 for the error

Figure 18: Typical Compensation Network

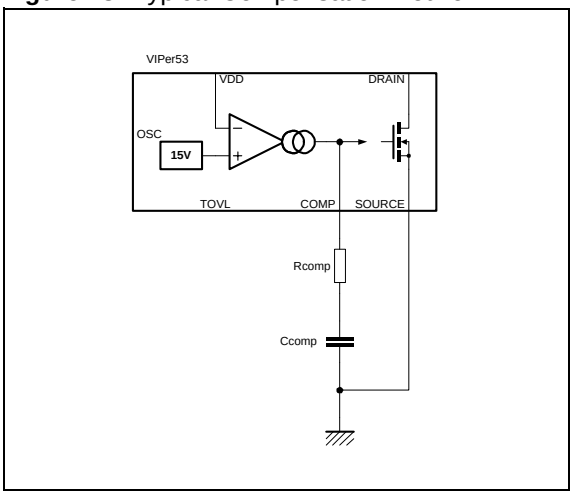
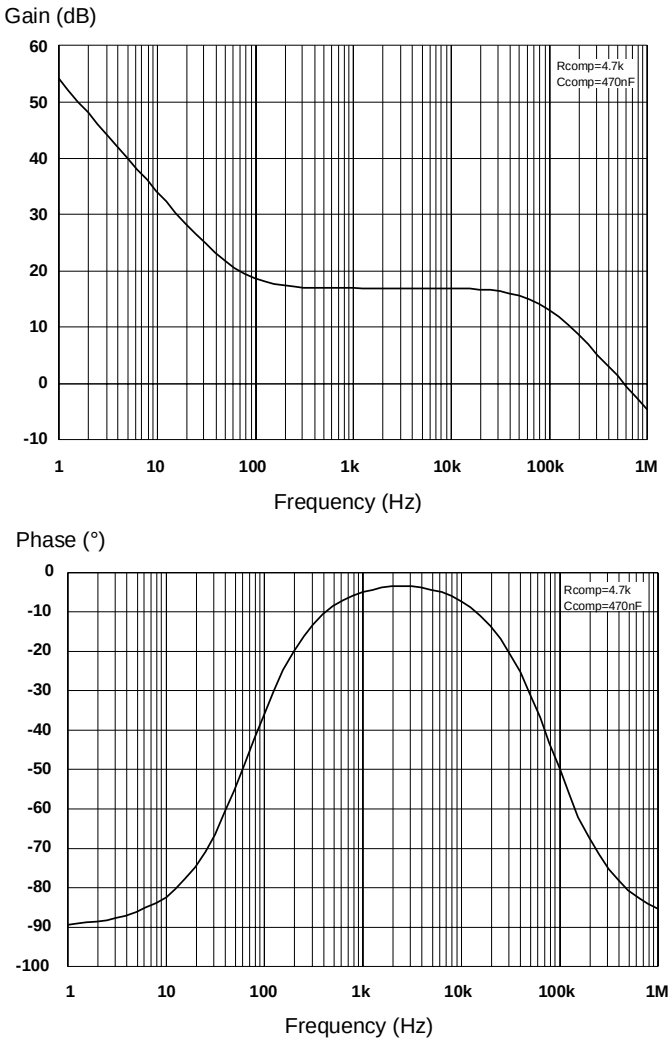


Figure 19: Typical Transfer Functions



amplifier transfer function for a typical set of values for C_{COMP} and R_{COMP}.

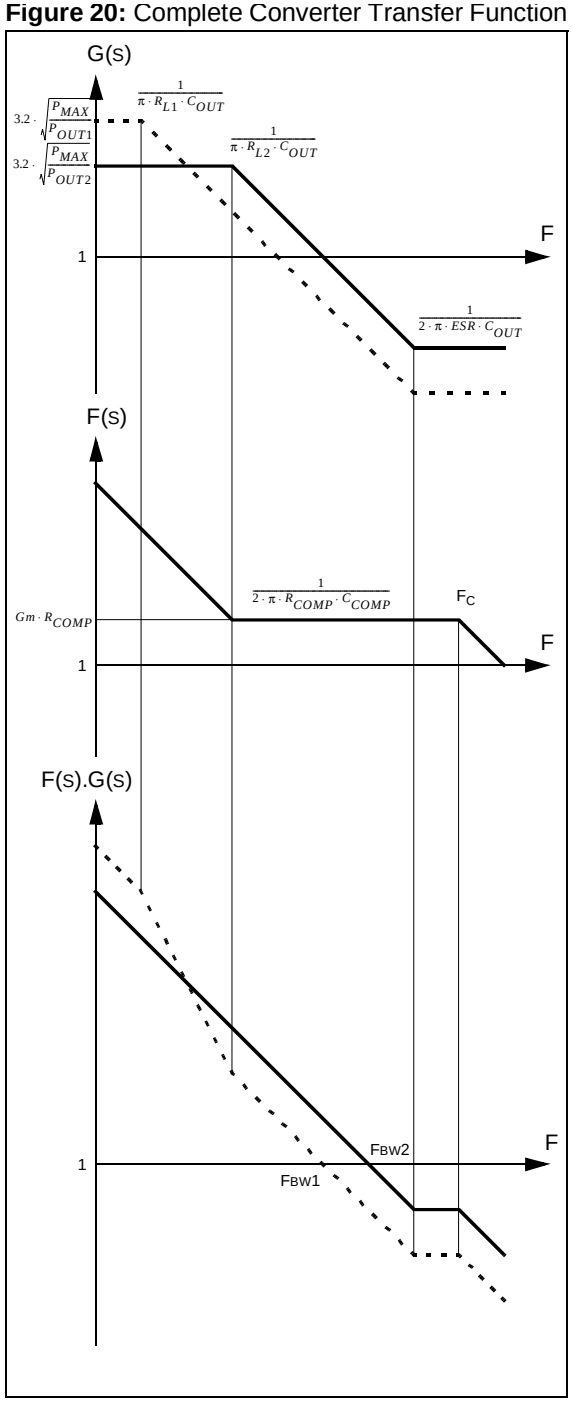
The complete converter open loop transfer function can be built from both power cell and error amplifier transfer functions. A theoretical example can be seen in figure 20 for a discontinuous mode flyback loaded by a simple resistor, regulated from primary side (no optocoupler, the internal error amplifier is fully used for regulation). A typical schematic corresponding to this situation can be seen on figure 14.

The transfer function of the power cell is represented as G(s) in figure 20. It exhibits a pole which depends on the output load and on the output capacitor value. As the load of a converter may change, two curves are shown for two different values of output resistance value, R_{L1} and R_{L2}. A zero at higher frequency values then appears, due to the output capacitor ESR. Note that the overall transfer function doesn't depend on the input voltage, thanks to the current mode control.

The error amplifier has a fixed behavior, similar to the one shown in figure 19. Its bandwidth is limited, in order to avoid injection of high frequency noise in the current mode section. A zero due to the R_{COMP}-C_{COMP} network is set at the same value as the maximum load R_{L2} pole.

The total transfer function is shown as F(s).G(s) at the bottom of figure 20. For maximum load (plain line), the load pole is exactly compensated by the zero of the error amplifier, and the result is a

Figure 20: Complete Converter Transfer Function



perfect first order decreasing slope until it reaches the zero of the output capacitor ESR. The error amplifier cut off then prevents definitely any further spurious noise or resonance from disturbing the regulation loop. The point where the complete transfer function has a unity gain is known as the regulation bandwidth and has a double interest:

– The higher it is the faster will be the reaction to an eventual load change, and the smaller will be the output voltage change.
– The phase shift in the complete system at this point has to be less than 135 ° to ensure a good stability. Generally, a first order gives 90 ° of phase shift, and 180 ° for a second order.

In figure 20, the unity gain is reached in a first order slope, so the stability is ensured.

The dynamic load regulation is improved by increasing the regulation bandwidth, but some limitations have to be respected: As the transfer function above the zero due the capacitor ESR is not reliable (The ESR itself is not well specified, and other parasitic effects may take place), the bandwidth should always be lower than the minimum of F_C and ESR zero.

As the highest bandwidth is obtained with the highest output power (Plain line with R_{L2} load in figure 20), the above criteria will be checked for this condition and allows to define the value of R_{COMP}, as the error amplifier gain depends only on this value for this frequency range. The following formula can be derived:

$$R_{COMP} = \sqrt{\frac{P_{OUT2}}{P_{MAX}}} \cdot \frac{F_{BW2} \cdot R_{L2} \cdot C_{OUT}}{Gm}$$

With: $P_{OUT2} = \frac{V_{OUT}^2}{R_{L2}}$

And: $P_{MAX} = \frac{1}{2} \cdot L_P \cdot I_{LIM}^2 \cdot F_{SW}$:

The lowest load gives another condition for stability: The frequency F_{BW1} must not encounter the second order slope generated by the load pole and the integrator part of the error amplifier. This condition can be met by adjusting the C_{COMP} value:

$$C_{COMP} > \frac{R_{L1} \cdot C_{OUT}}{6.3 \cdot Gm \cdot R_{COMP}^2} \cdot \sqrt{\frac{P_{OUT1}}{P_{MAX}}}$$

With: $P_{OUT1} = \frac{V_{OUT}^2}{R_{L1}}$

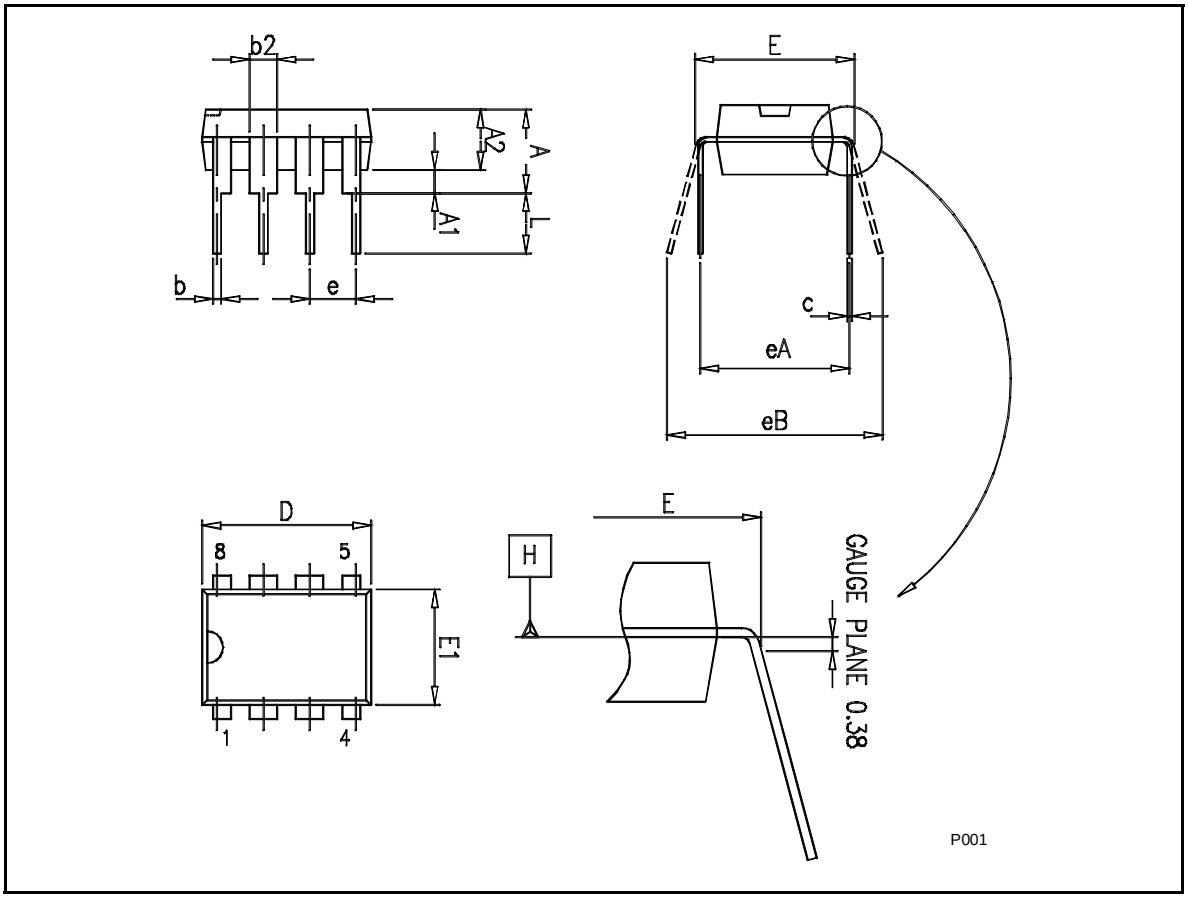
The above formula gives a minimum value for C_{COMP}. It can be then increased to provide a natural soft start function as this capacitor is charged by the error amplifier current capacity I_{COMPhi} at startup.

SOFTWARE IMPLEMENTATION

All the above considerations and some others are included in a design software which provides all the needed components around the VIPer device for a specified output configuration. This software is available in download on the ST internet site.

Plastic DIP-8 MECHANICAL DATA

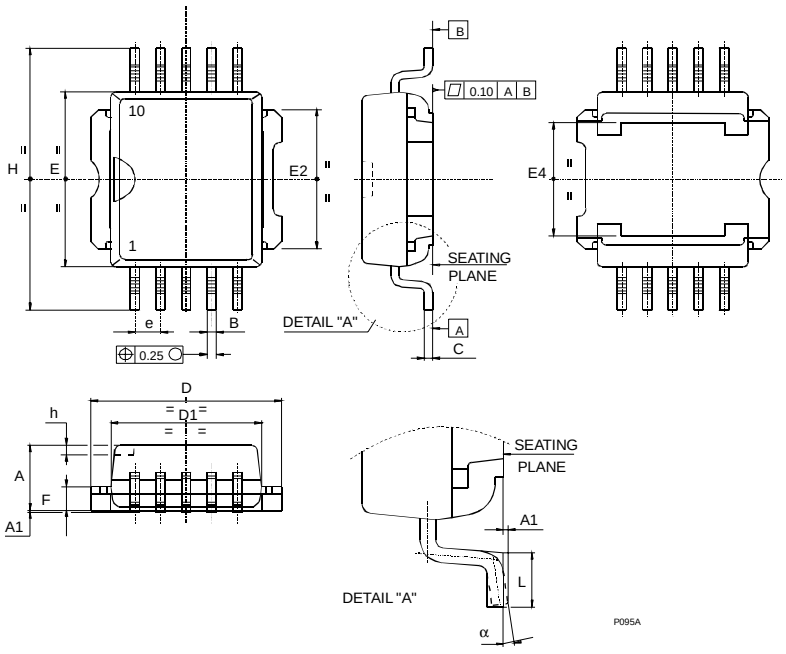
DIM.	mm.		
	MIN.	TYP	MAX.
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.26
E1	6.10	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81
Package Weight	Gr. 470		



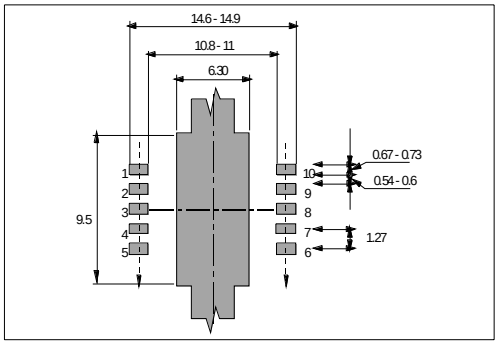
PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0º		8º	0º		8º
α (*)	2º		8º	2º		8º

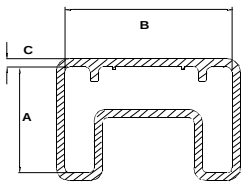
(*) Muar only POA P013P



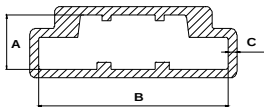
PowerSO-10™ SUGGESTED PAD LAYOUT



TUBE SHIPMENT (no suffix)



CASABLANCA

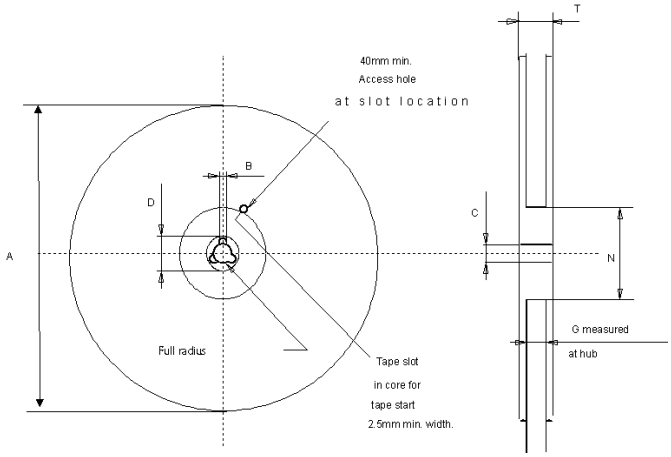


MUAR

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

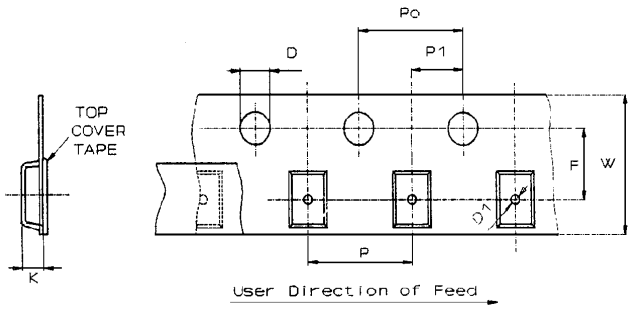
All dimensions are in mm.

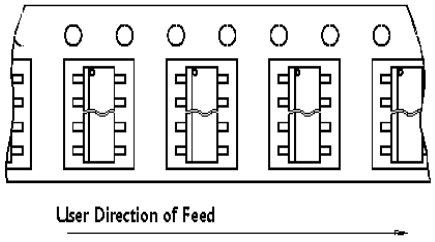
TAPE DIMENSIONS

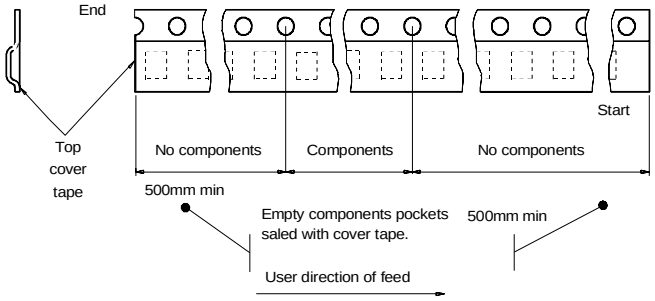
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

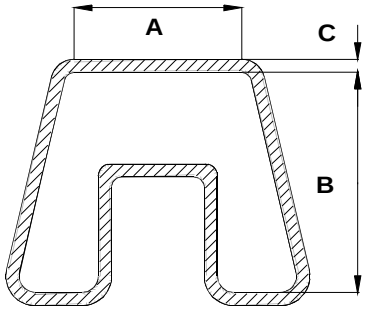
All dimensions are in mm.







DIP-8 TUBE SHIPMENT (no suffix)



Base Q.ty	20
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	8.4
B	11.2
C (± 0.1)	0.8

All dimensions are in mm.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may results from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.
The ST logo is a trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in ITALY- All Rights Reserved.

STMicroelectronics GROUP OF COMPANIES
Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com